

1 peripheral circuitry and pitch circuitry formed on the die relative
2 to the memory arrays; the peripheral circuitry electrically interconnecting
3 with the pins and including operably interconnected control and timing
4 circuitry, address and redundancy circuitry, data and test path circuitry,
5 and voltage supply circuitry which collectively enable full access to all
6 addressable memory cells of the memory arrays.

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10 ~~6.~~ (Amended) A 16M semiconductor memory device comprising:
11 a semiconductor die encapsulated in a package, the package having
12 an encapsulating body and electrically conductive interconnect pins
13 extending outwardly from the body;

14 a total of [no more than] from 16,000,000 to 17,000,000 functional
15 and operably addressable memory cells arranged in multiple memory
16 arrays formed on the die, the individual functional and operably
17 addressable memory cells occupying area on the die within the memory
18 arrays, the occupied area of all functional and addressable memory cells
19 on the die having a total combined area which is no greater than 14
20 mm²; and

21 peripheral circuitry and pitch circuitry formed on the die relative
22 to the memory arrays; the peripheral circuitry electrically interconnecting
23 with the pins and including operably interconnected control and timing
24 circuitry, address and redundancy circuitry, data and test path circuitry.

1 and voltage supply circuitry which collectively enable full access to all
2 addressable memory cells of the memory arrays.

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6 11. (Amended) A 4M semiconductor memory device comprising:
7 a semiconductor die encapsulated in a package, the package having
8 an encapsulating body and electrically conductive interconnect pins
9 extending outwardly from the body;

10 a total of [no more than] from 4,000,000 to 4,500,000 functional
11 and operably addressable memory cells arranged in multiple memory
12 arrays formed on the die, the individual functional and operably
13 addressable memory cells occupying area on the die within the memory
14 arrays, the occupied area of all functional and addressable memory cells
15 on the die having a total combined area which is no greater than 3.3
16 mm²; and

17 peripheral circuitry and pitch circuitry formed on the die relative
18 to the memory arrays; the peripheral circuitry electrically interconnecting
19 with the pins and including operably interconnected control and timing
20 circuitry, address and redundancy circuitry, data and test path circuitry,
21 and voltage supply circuitry which collectively enable full access to all
22 addressable memory cells of the memory arrays.

1 16. (Amended) A 64M semiconductor memory device comprising:
2 a semiconductor die encapsulated in a package, the package having
3 an encapsulating body and electrically conductive interconnect pins
4 extending outwardly from the body;

5 a total of [no more than] from 64,000,000 to 68,000,000 functional
6 and operably addressable memory cells arranged in multiple memory
7 arrays formed on the die, at least one of the memory arrays containing
8 at least 100 square microns of continuous die surface area having at
9 least 128 of the functional and operably addressable memory cells; and

10 peripheral circuitry and pitch circuitry formed on the die relative
11 to the memory arrays; the peripheral circuitry electrically interconnecting
12 with the pins and including operably interconnected control and timing
13 circuitry, address and redundancy circuitry, data and test path circuitry,
14 and voltage supply circuitry which collectively enable full access to all
15 addressable memory cells of the memory arrays.

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19 18. (Amended) A 16M semiconductor memory device comprising:
20 a semiconductor die encapsulated in a package, the package having
21 an encapsulating body and electrically conductive interconnect pins
22 extending outwardly from the body;

23 a total of [no more than] from 16,000,000 to 17,000,000 functional
24 and operably addressable memory cells arranged in multiple memory

1 arrays formed on the die, at least one of the memory arrays containing
2 at least 100 square microns of continuous die surface area having at
3 least 128 of the functional and operably addressable memory cells; and
4 peripheral circuitry and pitch circuitry formed on the die relative
5 to the memory arrays; the peripheral circuitry electrically interconnecting
6 with the pins and including operably interconnected control and timing
7 circuitry, address and redundancy circuitry, data and test path circuitry,
8 and voltage supply circuitry which collectively enable full access to all
9 addressable memory cells of the memory arrays.

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13 20. (Amended) A 4M semiconductor memory device comprising:
14 a semiconductor die encapsulated in a package, the package having
15 an encapsulating body and electrically conductive interconnect pins
16 extending outwardly from the body;

17 a total of [no more than] from 4,000,000 to 4,500,000 functional
18 and operably addressable memory cells arranged in multiple memory
19 arrays formed on the die, at least one of the memory arrays containing
20 at least 100 square microns of continuous die surface area having at
21 least 128 of the functional and operably addressable memory cells; and
22 peripheral circuitry and pitch circuitry formed on the die relative
23 to the memory arrays; the peripheral circuitry electrically interconnecting
24 with the pins and including operably interconnected control and timing

1 circuitry, address and redundancy circuitry, data and test path circuitry,
2 and voltage supply circuitry which collectively enable full access to all
3 addressable memory cells of the memory arrays.
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